

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Shunpei YAMAZAKI)
Serial No. 09/583,087)
Filed: September 5, 2000)
For: ELECTRO-OPTICAL DEVICE)
AND METHOD FOR)
MANUFACTURING THE SAME)

Art Unit: 2815
Examiner: J. Jackson, Jr.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with
The United States Postal Service with sufficient postage as First
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Rose M. Sichel

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, DC 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be considered by the Examiner and made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

In accordance with 37 C.F.R. § 1.97(e), it is certified that either (1) each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement, or (2) no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign patent application and no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this information disclosure statement.

U.S. Patent 4,942,441 is in the family of JP 62-229873.

JP 01-272146 was cited by the Japanese Patent Office for asserting that in an active matrix liquid crystal device, it would have been easy to use a P-channel thin film

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transistor and an N-channel thin film transistor connected to each other through a transparent conductive film.

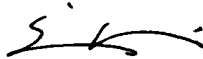
JP 02-216129, JP 03-255425 Japan Utility Model Laid Open No. 03-081922 and Japan Utility Model Laid Open No. 03-071382 were cited by the Japanese Patent Office for asserting that in a well known active matrix liquid crystal display device, it was well known to connect another IC by a COG method or a TAB method.

The Integrated Circuit Engineering (1) article was cited by the Japanese Patent Office for showing it is well known that an N-channel MOS transistor is capable of driving at a higher speed since it uses electrons as carriers.

The Integrated Circuit Engineering (2) article was cited by the Japanese Patent Office for showing that a circuit constituted with complementary MOS transistors is formed by using a plurality of MOS transistors having a same channel type.

The Commissioner is hereby authorized to charge any fees connected with this filing which may be required now, or credit any overpayment to Deposit Account No. 50-2280.

Respectfully submitted,



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